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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,242	01/16/2004	Shi-dong Zhou	X-1401 US	7069

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,242	ZHOU, SHI-DONG	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-17 and 19-30* is/are allowed.

6)☒ Claim(s) *31-41 and 43-53* is/are rejected.

7)☒ Claim(s) *42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Upon further consideration of the application, the indication of allowance for claims 31-53 is withdrawn and the new ground(s) of rejection is set forth below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 31-41 and 43-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff et al. (U. S. PAT. 5,550,782) in view of Hamada et al. (U. S. PAT. 6,373,291).

In claim 31, Cliff et al. teaches all claimed features in Fig. 9, an integrated circuit (IC), comprising: one or more configurable elements (20s); with the exception of teaching means for selectively providing either a first hardwired configuration bit or a second hardwired configuration bit to the one or more configurable elements in response to a select signal. However, Hamada et al. teaches in Fig. 2B, means (PT) for selectively providing either a first hardwired configuration bit (A) or a second hardwired configuration bit (B) to the one or more configurable elements (coupled to Z) in response to a select signal (S).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to implement means (PT) for selectively providing hardwired configuration bits of Hamada et al. to control to configurable elements (20s) of Cliff et all, in order to reduce power consumption in the integrated circuit.

In claim 32, Hamada et al. further teaches the IC of claim 31, wherein the means (PT) for selectively providing does not include any memory cells (no memory cells).

In claim 33, Hamada et al. further teaches the IC of claim 31, wherein the first and second hardwired configuration bits (A, B) configure the one or more configurable elements to different configuration states (logic 1 or logic 0).

In claim 34, Hamada et al. further teaches the IC of claim 33, wherein the first hardwired configuration bit (A) comprises a supply voltage (logic 1) and the second hardwired configuration bit (B) comprises ground potential (logic 0).

In claim 35, Hamada et al. further teaches the IC of claim 31, wherein the first and second hardwired configuration bits (A, B) configure the one or more configurable elements to the same configuration state (same logic value).

In claim 36, Hamada et al. further teaches the IC of claim 33, wherein the first and second hardwired configuration bits comprises a supply voltage (logic 1).

In claim 37, Hamada et al. further teaches the IC of claim 33, wherein the first and second hardwired configuration bits comprise ground potential (logic 0).

In claim 38, Hamada et al. further teaches the IC of claim 31, wherein the means (PT) for selectively providing comprises a multiplexer (as seen in Fig. 2B).

In claim 39, Hamada et al. further teaches the IC of claim 31, wherein the means (PT) for selectively providing comprises a first transistor (NM2) connected between the first hardwired configuration bit (A) and the configurable element (coupled to Z) and having a gate responsive to the select signal (S); and a second transistor (NM1)

connected between the second hardwired configuration bit (B) and the configurable element and having a gate responsive to a complement of the select signal (inverted S).

In claim 40, Hamada et al. further teaches the IC of claim 31, wherein the select signal is generated within the IC.

In claim 41, Hamada et al. further teaches the IC of claim 31; with the exception of teaching wherein the select signal comprises an external provided to an input pin of the IC. However, the selected signal can be either internal or external signal of the IC.

Claims 43-47 correspond to detailed circuitry already discussed similarly with regard to claims 31-41.

Method claims 48-53 correspond to detailed circuitry already discussed similarly with regard to claims 31-41.

4. Claim 42 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 1-17 and 19-30 appear to comprise allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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VIBOL TAN
PRIMARY EXAMINER